ABSTRACT

A semiconductor device having high tensile stress. The semiconductor device comprises a substrate having a source region and a drain region. Each of the source region and the drain region includes a plurality of separated source sections and drain sections, respectively. A shallow trench isolation (STI) region is formed between two separated source sections of the source region and between two separated drain sections of the drain region. A gate stack is formed on the substrate. A tensile inducing layer is formed over the substrate. The tensile inducing layer covers the STI regions, the source region, the drain region, and the gate stack. The tensile inducing layer is an insulation capable of causing tensile stress in the substrate.